Please delete the paragraph beginning at page 1, line 16 and replace it with the following:

The present invention aims at implementing a monolithic protection circuit capable of establishing a short-circuit between each conductor of a line and a ground when the voltage on this conductor exceeds a determined positive threshold or becomes lower than a predetermined negative threshold.

Please add the following heading before the fourth paragraph on page 1, line 16:

Summary Of The Invention

Please delete the paragraph beginning at page 2, line 13 and replace it with the following:

To achieve these objects, the present invention provides a monolithic component that protects against line overvoltages greater than a determined positive threshold or lower than a determined negative threshold, including in antiparallel a cathode-gate thyristor and an anode-gate thyristor connected between a first terminal of the line to be protected and a reference voltage, the gate of the cathode-gate thyristor being connected to a negative threshold voltage via a gate current amplification transistor, the gate of the anode-gate thyristor being connected to a positive threshold voltage. The monolithic component is made in a substrate of the first conductivity type divided into wells separated by isolating walls, the lower surfaces of which are coated with insulating layers, the lower surface of the substrate being uniformly coated with a metallization. The gate current amplification transistor of the cathode-gate thyristor is made in vertical form in a first well. The cathode-gate thyristor is implemented in vertical form in a second well. The anode-gate thyristor is implemented in vertical form in a third well. The lower surface metallization links up the collector of the transistor, the anode of the cathode-gate thyristor, and the cathode of the anode-gate thyristor. A first front surface metallization connects the cathode of the cathode-gate thyristor to the anode of the anode-gate thyristor. A second front surface metallization connects the gate of the cathode-gate thyristor to the emitter of the transistor. A third front surface metallization is in contact with the gate of the anode-gate thyristor.

Please delete the paragraph beginning at page 3, line 9 and replace it with the following:

According to an embodiment of the present invention, the gate of the cathode-gate thyristor is connected to a second terminal of the line to be protected associated with the anode-gate thyristor, this transistor, of PNP type, being formed on the upper surface of the component, the collector region extending via isolating walls towards the lower surface and being in contact with the lower surface metallization.

Please add the following heading before the third paragraph on page 3, line 16:

Brief Description Of The Drawings

Please add the following heading before the last paragraph on page 3, line 33:

Detailed Description

Please delete the paragraph beginning at page 4, line 27 and replace it with the following:

- If a negative overvoltage lower than voltage –V occurs on conductor L1, cathode-gate thyristor Th1 turns on and the negative overvoltage flows towards the ground. Transistor T1 increases the triggering sensitivity by acting as a gate amplifier.

Please delete the paragraph beginning at page 5, line 1 and replace it with the following:

A device that protects against overvoltages and overcurrents on conductor L1 has thus effectively been obtained. The lower portion of the circuit performs the same function for conductor L2.

Please delete the paragraph beginning at page 5, line 17 and replace it with the following:

The component of Fig. 1B is formed from an N-type substrate 1 divided into three wells by isolating walls 3 and 4. Each isolating wall is formed by a P-type drive-in extending from the upper and lower surfaces of the layer, with these diffusions joining substantially at the middle of the wafer. The component is performed in a semiconductor power component technology in which a single metallization M1 covers the entire lower surface or rear surface of the component. According to an aspect of the present invention, a technology in which the apparent portion of

each isolating wall on the lower surface side is insulated by an insulating layer is used. Reference 5 designates an insulating layer, currently silicon oxide, formed under the lower surface of isolating wall 3 and reference 6 designates an insulating layer formed under the lower surface of isolating wall 4.

Please delete the paragraph beginning at page 5, line 31 and replace it with the following:

Transistor T1 is formed in the left-hand well. This transistor is of vertical type and includes on the upper surface side a P-type base region 10 containing an N-type emitter region 11. On the lower surface side is formed an N^+-type region 12 forming the collector contact recovered by metallization M1. It should be noted that insulating layer 5 extends so that metallization M1 contacts N region 12 and not substrate 1 of the well. An advantage of implementing this transistor in vertical form is that it can easily withstand relatively high voltages (voltage –V is for example -50 V). Further, the connection between the collector of this transistor and the anode of cathode-gate thyristor Th1 is performed in a particularly simple and efficient way by the rear surface metallization. Further, transistor T1 has a high gain (on the order of 80 to 200) which results in a particularly low current to be supplied by battery –V upon each triggering.

Please delete the paragraph beginning at page 6, line 11 and replace it with the following:

Cathode-gate thyristor Th1 is formed in the central well of Fig. 1B. It is implemented in vertical form. It includes on the lower surface side an anode region 30 and on the upper surface side a P-type region 31 and an N-type cathode region 32, currently provided with emitter short-circuits. It should be noted that insulating regions 5 and 6 extend to P region 30 so that metallization M1 does not contact the N-type central well.

Please delete the paragraph beginning at page 6, line 18 and replace it with the following:

In the right-hand well of Fig. 1B are formed anode-gate thyristor Th2 and diode D1. Thyristor Th2 is made in the same way as thyristor Th1 in vertical form. It includes on the lower surface side an N cathode region 40, and on the upper surface side a deep lightly-doped P-type region 42 (made at the same time as anode region 30 of thyristor Th1) in which are formed an N-

type region 43 and a P-type anode region 44. Conventionally, the anode region is provided with emitter short-circuits. Diode D1 is formed in P-type region 42 and includes in this region an N-type region 45 forming its cathode and a P-type region 46 forming its anode. This diode is a lateral diode.

Please delete the paragraph beginning at page 7, line 20 and replace it with the following:

Fig. 2A shows an alternative of the circuit of Fig. 1A. Elements T1, Th1, Th2, T1′, Th1′, Th2′ reappear therein. The difference with Fig. 1A is that the gate of anode-gate thyristor Th2 is not connected to the gate of cathode-gate thyristor Th1 and is directly connected, as well as the gate of anode-gate thyristor Th2′ to positive reference voltage +V. This circuit is simpler but does not protect against positive overcurrents. It however has the advantage that the anode-gate thyristor is particularly sensitive due to the absence of anode short-circuits.

Please delete the paragraph beginning at page 8, line 8 and replace it with the following:

Fig. 3A shows another alternative of the circuit according to the present invention. This time, the structure is completely symmetrical, that is, anode-gate thyristor Th2 is, like cathode-gate thyristor Th1, associated with a gate current amplification transistor. This transistor is designated with reference T2 for thyristor Th2 and with reference T2′ for thyristor Th2′. Transistors T2 and T2′ are PNP transistors while transistors T1 and T1′ are NPN transistors.

Please delete the paragraph beginning at page 8, line 16 and replace it with the following:

An implementation according to the present invention in monolithic form of the circuit of Fig. 3A appears in a simplified cross-section in Fig. 3B. Transistor T1 and transistor Th1 are implemented in the same way as in the embodiments of Figs. 1B and 2B. Thyristor Th2 is implemented in the same way as that of Fig. 1B or of Fig. 2B according to the sensitivity desired for this thyristor. Transistor T2 is implemented between the wells containing thyristors Th1 and Th2. The collector of this transistor is formed of a P-type layer 61 deeply diffused from the upper surface. Region 61 is surrounded with a P-type drive-in 62 which joins a P-type region 63 formed from the lower surface and on which is recovered the collector contact by metallization M1. Inside collector region 61 are formed a base region 64 and a P-type emitter region 65.